

1 Claims

2 1. Device to measure individual cell voltages (U_z) of the
3 cells (Z_1 to Z_n) in a cell stack (ZS) of an energy
4 accumulator, especially of an energy accumulator in a motor
5 vehicle electrical system,

6

7 characterized in that

8

9 a series circuit of two diodes ($D_{1a}-D_{1b}$ to $D_{na}-D_{nb}$), which
10 conduct current in the direction from the minus pole to the
11 plus pole of the cell, is arranged in parallel to each cell
12 (Z_1 to Z_n),

13

14 a changeover switch is provided which features a number of
15 terminals assigned to switch positions corresponding to the
16 number of cells (Z) of the cell stack (ZS), which are
17 connected via a capacitor (C_1 to C_n) in each case to the
18 connection points of the diodes ($D_{1a}-D_{1b}$ to $D_{na}-D_{nb}$)
19 assigned to the cells,

20

21 a reference circuit (REF) is provided which features two
22 series-connected diodes (D_3 , D_4), with the anode of one
23 diode (D_4) being connected to reference potential (GND) and
24 to the cathode of the other diode (D_3).

25

1 a differential amplifier (Diff1) is provided, of which the
2 non-inverted input is connected to the output of the
3 changeover switch (UM) and of which the inverted input is
4 connected via a capacitor (C3) to the connection point of
5 the two diodes (D3, D4),

6

7 a controlled rectifier (GLR) is provided of which the input
8 is connected to the output of the differential amplifier
9 (Diff1) and at the output of which a direct current ($V=$)
10 related to reference potential (GND) proportional to the
11 cell voltage (U_z) of the cells selected in each case using
12 the changeover switch (UM) can be tapped off.

13

14 a first controlled alternating current source (I1) is
15 provided is arranged between the non-inverting input of the
16 differential amplifier (Diff1) and reference potential (GND)

17

18 a second controlled alternating current source (I2) is
19 provided which is arranged between the inverting input of
20 the differential amplifier (Diff2) and reference potential
21 (GND)

22

23 a clock control (ST) is provided which features an
24 oscillator (OSZ) which outputs an oscillator clock signal
25 (T1) and features a frequency divider (DIV) which outputs a

1 divider signal (T2), with the two alternating current
2 sources (I1, I2) and the rectifier (GLR) being controlled by
3 the oscillator clock (T1) and the changeover switch (UM)
4 being controlled by the divider signal (T2).

5

6 2. Device in accordance with claim 1, characterized in that
7 the rectifier (GLR) is embodied as a synchronous demodulator
8 (Amp1, Diff2) controlled by the oscillator clock (T1).

9

10 3. Method for operating the device in accordance with claim
11 1,

12

13 characterized in that

14

15 to measure the cell voltage (Uz) of a specific cell (Z1 to
16 Zn) of the cell stack (ZS) a first, square-wave alternating
17 current of a specific frequency (T1) and amplitude is
18 injected into the capacitor (C1 to Cn) assigned to the cell,
19 which produces an alternating voltage (V1) which corresponds
20 to the cell voltage (Uz), multiplied by the on-state
21 voltages (Ud) of the two diodes (D1a-D1b to Dna-Dnb) lying
22 in parallel to the cell (Uz).

23

24 an alternating current which is equal in frequency and
25 amplitude to the first square-wave alternating current is

1 injected into the capacitor (C3) assigned to the reference
2 circuit (REF), which produces an alternating voltage (V2)
3 related to ground (reference potential GND) which
4 corresponds to the on-state current ($2 \cdot I_{Du}$) of the two diodes
5 (D3, D4) assigned to the reference circuit (REF),

6
7 the difference ($V1 - V2$) between the two alternating voltages
8 ($V1$, $V2$) is formed, with an alternating voltage
9 corresponding to the cell voltage (U_z) arising, and

10
11 the alternating voltage corresponding to the cell voltage
12 (U_z) is rectified which produces a direct voltage ($V=$)
13 corresponding to the cell voltage (U_z) related to ground
14 (reference potential GND).

15
16 4. Method in accordance with one of the previous claims,
17 characterized in that this method is applied consecutively
18 to all cells ($Z1$ to Zn) of the cell stack (ZS).

19
20 5. Method in accordance with claim 3 or 4, characterized in
21 that the frequency (clock frequency $T1$) of the alternating
22 currents injected into the capacitors ($C1$ to Cn and $C3$) is
23 selected to be high enough so that the capacitors do not
24 significantly charge or discharge during the oscillation
25 period.

1 6. Method in accordance with claim 3 or 4, characterized in
2 that the amplitudes of the alternating currents injected
3 into the capacitors (C1 to Cn and C3) lie within the μA
4 range.

5

6 7. Method in accordance with Claim 3 or 4, characterized in
7 that the direct current voltage ($V=$) corresponding to the
8 cell current (U_z) of each cell ($Z1$ to Zn) related to ground
9 (reference potential GND) is subjected to a limit value
10 comparison at the upper and a lower limit value, in which
11 case exceeding the upper limit value indicates an
12 overvoltage of the cell and falling below the lower limit
13 value indicates a short-circuit the cell.

14

15 8. Method in accordance with claim 3 or 4, characterized in
16 that the direct current voltage values ($V=$) corresponding to
17 the cell voltages (U_z) of each cell ($Z1$ to Zn) related to
18 ground (reference potential GND) are stored, in which case
19 during charge balancing, the slow balancing of individual
20 cell voltages (U_z) can be detected and the termination of
21 the charging or discharging process can be defined as well
22 as a long-term supervision of each individual cell ($Z1$ to
23 Zn) for a drop in the capacitance or an increase in the
24 self-discharge or the internal resistance.